

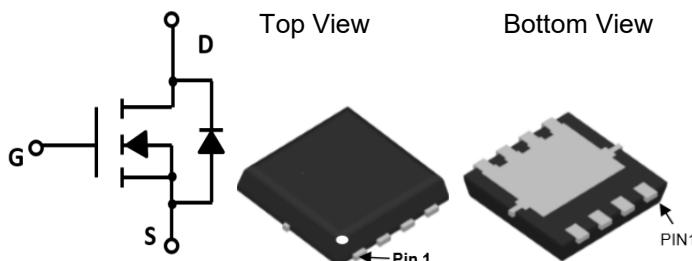
Description

The CMN6008GF5 is the N-Channel enhancement mode power field effect transistors with high cell density, trench technology. This high density process and design have been optimized switching performance and especially tailored to minimize on-state resistance.

Features

- V_{DS}: 60V
- I_D: 59A
- R_{DS(on)} (@V_{GS}=10V) : < 7.5mΩ
- R_{DS(on)} (@V_{GS}=4.5V) : < 10mΩ
- High density cell design for extremely low R_{DS(on)}
- Excellent on-resistance and DC current capability

Equivalent Circuit and Pin Configuration



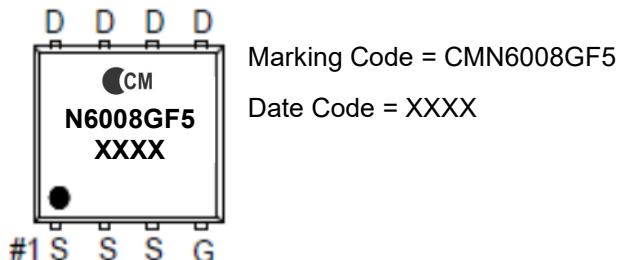
Absolute Maximum Ratings (TA=25 °C unless otherwise noted)

Parameter	Symbol	Maximum	Unit
Drain-source Voltage	V _{DS}	60	V
Gate-source Voltage	V _{GS}	±20	V
Drain Current ⁽¹⁾⁽⁶⁾	I _D	59	A
		37	A
	I _D	17	A
		11	A
Pulsed Drain Current ⁽³⁾	I _{DM}	216	A
Total Power Dissipation ⁽⁴⁾	P _D	41	W
		4.1	W
Thermal Resistance Junction-to-Ambient ⁽²⁾⁽⁵⁾	R _{θJA}	30	°C/W
Thermal Resistance Junction-to-Case	R _{θJC}	3	°C/W
Junction and Storage Temperature Range	T _{J,TSTG}	-55 to +150	°C

Applications

- Battery management
- Power management
- Load switch

Marking Information



Ordering Information

Part Number	Packaging	Reel Size
CMN6008GF5	5000/Tape & Reel	13 inch

Electrical Characteristics (T_J=25 °C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BVDSS	V _{GS} =0V, I _D =250μA	60			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V, V _{GS} =0V, T _C =25°C			1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1		3	V
Static Drain-Source on-Resistance	R _{D(on)}	V _{GS} =10V, I _D =15A		5.5	7.5	mΩ
		V _{GS} =4.5V, I _D =10A		7	10	
Diode Forward Voltage	V _{SD}	I _S =20A, V _{GS} =0V			1.2	V
Maximum Body-Diode Continuous Current	I _S				59	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =30V, V _{GS} =0V, f=1MHz		1920		pF
Output Capacitance	C _{oss}			430		
Reverse Transfer Capacitance	C _{rss}			3		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =30V, I _D =25A		32		nC
Gate Source Charge	Q _{gs}			5		
Gate Drain Charge	Q _{gd}			7.5		
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DS} =30V, R _L =10Ω, R _{GEN} =3Ω		18.4		ns
Turn-on Rise Time	t _r			3.3		
Turn-off Delay Time	t _{D(off)}			46		
Turn-off Fall Time	t _f			13		

Noted: (1) Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

- (2) The value of R_{θJA} is measured with the device mounted on lin2 FR-4 board with 2oz.Copper,in a still air environment with T_A =25°C.The Power dissipation PDSM is based on R_{θJA} t≤10s and the maximum allowed junction temperature of 150°C.The value in any given application depends on the user's specific board design.
- (3) Single pulse width limited by junction temperature T_{J(MAX)} = 150°C.
- (4) The power dissipation PD is based on T_{J(MAX)} = 150°C,using junction-to-case thermal resistance, and is more useful in setting the upper Dissipation limit for cases where additional heatsinking is used.
- (5) The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJA} and case to ambient.
- (6) Drain current limited by maximum junction temperature.

Typical Performance Characteristics

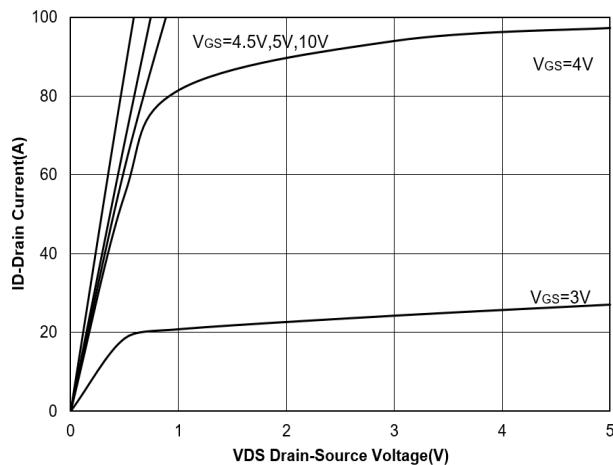


Figure 1. Output Characteristics

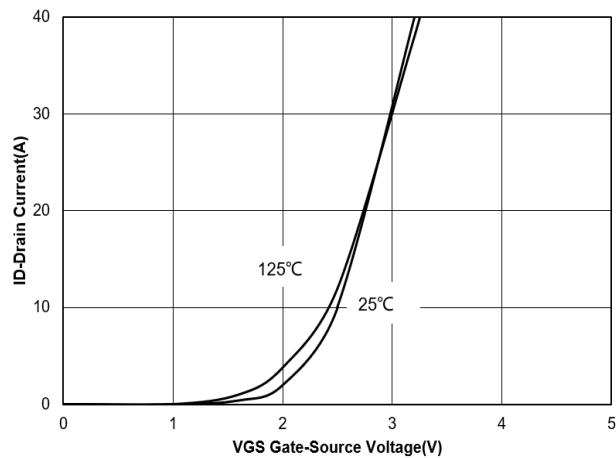


Figure 2. Transfer Characteristics

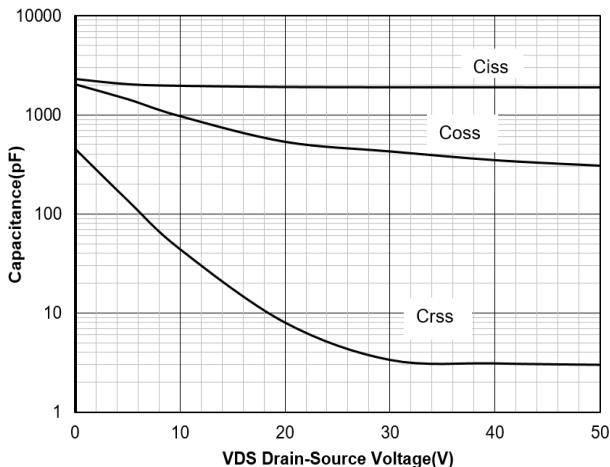


Figure 3. Capacitance Characteristics

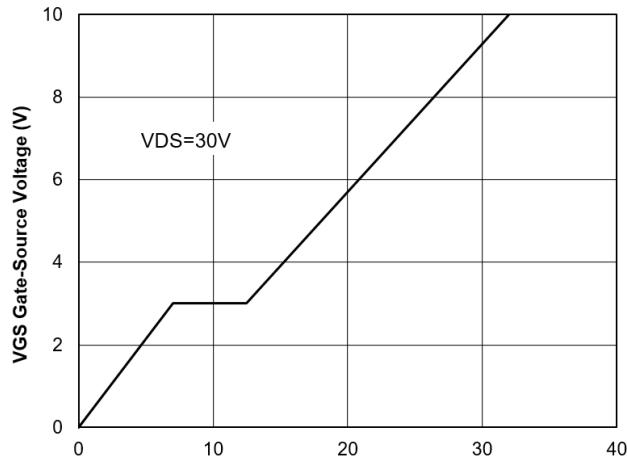


Figure 4. Gate Charge

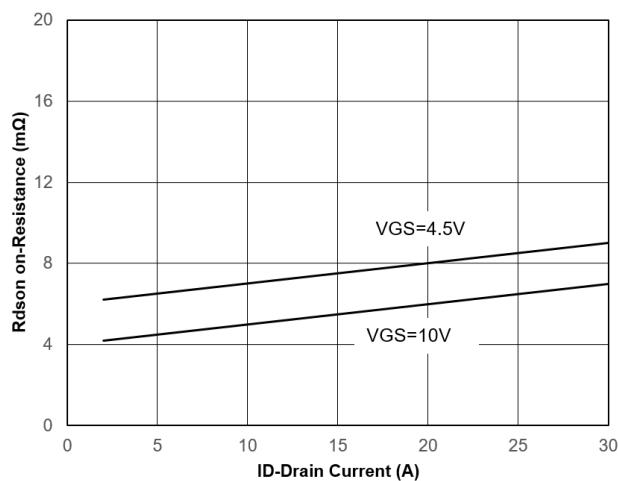


Figure 5. Drain-Source on Resistance

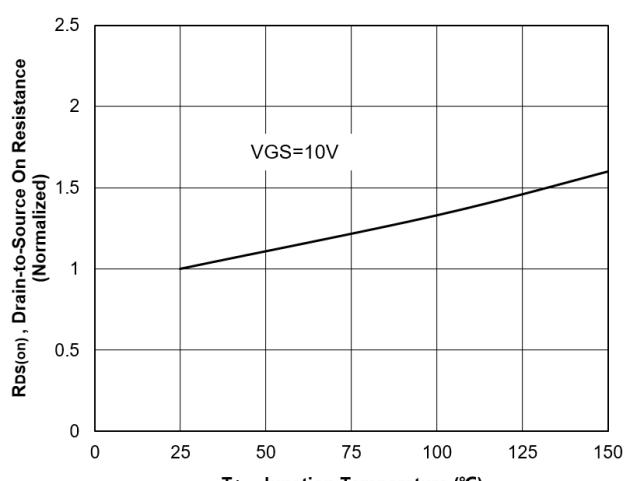


Figure 6. Normalized On-Resistance Vs. Temperature

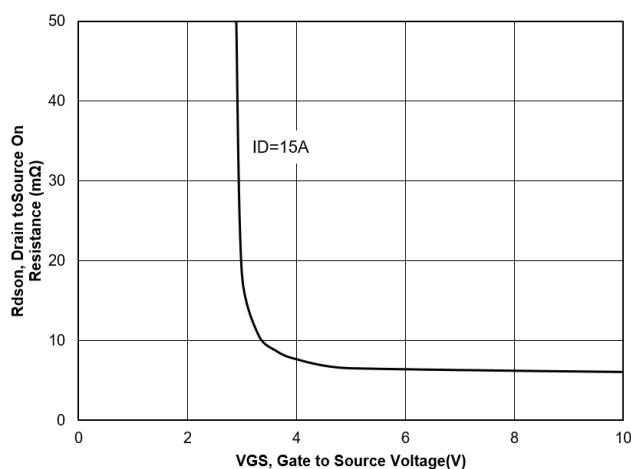


Figure 7. Typical Drain to Source ON Resistance
VS Gate Voltage and Drain Current

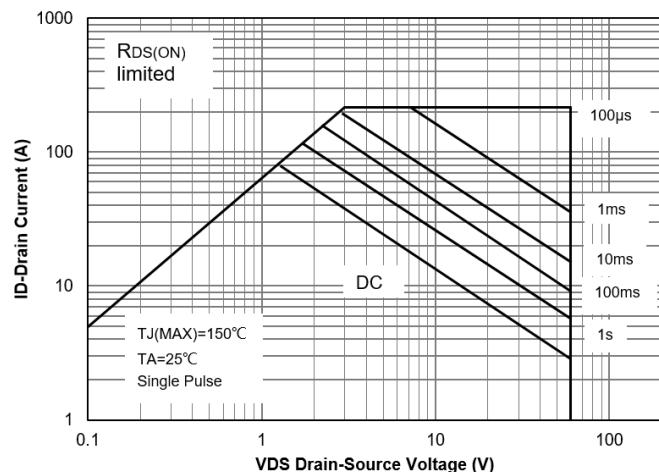


Figure 8. Safe Operation Area

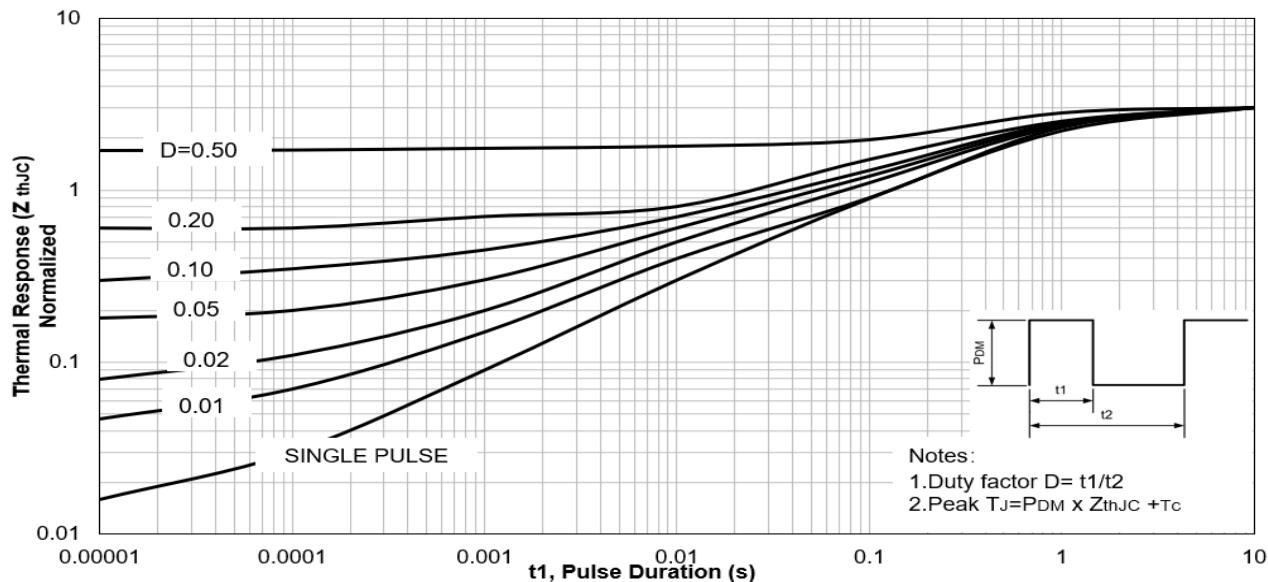


Figure 9. Maximum Effective Transient Thermal Impedance, Junction-to-Case

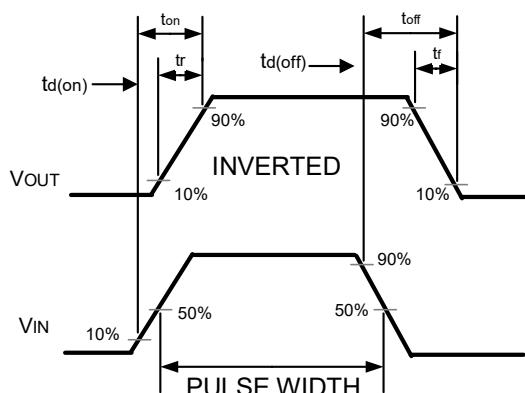
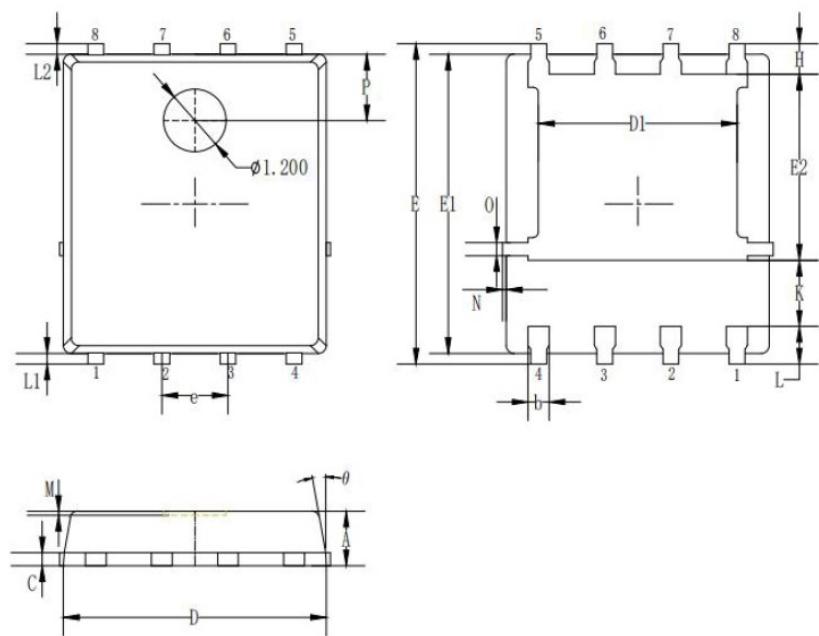


Figure 10. Switching wave

PDFN 5X6 Package Outline Drawing



Symbol	Millimeters		
	Min.	Nom.	Max.
A	0.90	1.05	1.20
b	0.35	0.40	0.50
c	0.20	0.25	0.35
D	4.90	5.05	5.20
D1	3.72	3.82	3.92
E	6.00	6.15	6.30
E1	5.60	5.75	5.90
E2	3.47	3.57	3.67
e	1.27 BSC		
H	0.48	0.58	0.68
K	1.17	1.27	1.37
L	0.64	0.74	0.84
L1/L2	0.20 REF		
θ	8°	10°	12°
M	0.08 REF		
N	0	--	0.15
O	0.25 REF		
P	1.28 REF		

Contact Information

Applied Power Microelectronics Inc.

Website: <http://www.appliedpowermicro.com>

Email: sales@appliedpowermicro.com

Phone: +86 (0519) 8399 3606